DERWENT-ACC-NO: **2001-439033**

DERWENT-WEEK: 200147

TITLE: Semiconductor device with trench isolation layer and manufacturing method thereof

INVENTOR: JANG, H S

PATENT-ASSIGNEE: SAMSUNG ELECTRONICS CO LTD[SMSU]

PRIORITY-DATA: 1999KR-0022703 (June 17, 1999)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2001002746 A	January 15, 2001	N/A	001	H01L 021/76

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
KR2001002746A	N/A	1999KR-0022703	June 17, 1999

INT-CL (IPC): H01L021/76

ABSTRACTED-PUB-NO: KR2001002746A

BASIC-ABSTRACT:

NOVELTY - A semiconductor device and a manufacturing method thereof are to prevent from degrading of a function of a trench isolation layer by an oxide recess thus to improve a reliance of a semiconductor device.

DETAILED DESCRIPTION - A manufacturing method comprises the steps of: forming
an etching protecting pattern which is formed by serially depositing a pad
oxide layer and a hard mask layer on an active region of a semiconductor
substrate(30); forming a trench(38) for isolation of the device on a field
region of the semiconductor substrate by an isotropic etching using the etching
protection pattern; depositing an isolation substance to fill the trench;
forming a **trench isolation** layer(40) flattened by chemical mechanical polishing
the isolation substance until the etching protection pattern being exposed;
removing the etching protection pattern; and selectively performing **epitaxial**
growth a **silicon** layer(42) to fill an oxide recess.

CHOSEN-DRAWING: Dwg.1/10

DERWENT-CLASS: U11

EPI-CODES: U11-C08A2;

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Basic Abstract Text - ABTX (2):
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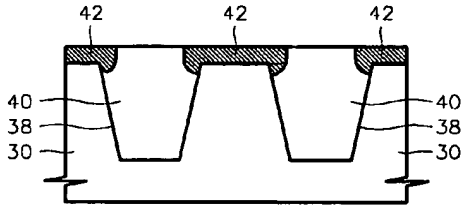
Derwent Accession Number - NRAN (1):
2001-439033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